(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 549 165 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92311063.9**

(22) Date of filing: **03.12.92**

(51) Int. Cl.5: **H03K 17/94**, H03K 17/28

(30) Priority: **23.12.91 US 813113**

(43) Date of publication of application: **30.06.93 Bulletin 93/26**

(84) Designated Contracting States: **DE FR GB NL**

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(54) Power conserving integrated circuit.

(57) A power conserving integrated circuit (20) is coupled to its external power supply (28) only in response to an external event sensed by closure of a switch (30). An initial power connection is made by a transistor (34) in the circuit (22) in response to the external event. After the initial power connection, the transistor (34) remains conducting so as to couple the power supply (28) to the integrated circuit (22) for a predetermined period of time sufficient for a function (40) to be executed by the integrated circuit. The initial power connection is detected by an activity monitor (37) which in response resets a down counter (38) that, through a connection (39) to the transistor (34), holds the transistor (34) in its conducting state until the counter (38) finishes counting clock pulses. The connection is then terminated and is not re-initiated until another external event. Therefore, power is consumed only when necessary, thereby preserving the power source (28).

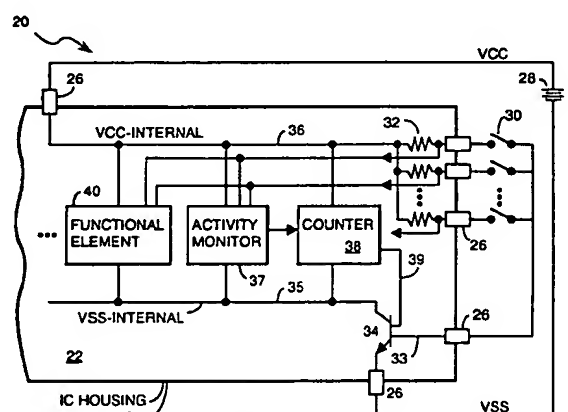

FIGURE 1

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This invention generally relates to minimizing the power consumption of an integrated circuit. More particularly, this invention relates to an integrated circuit which conserves power by utilizing power only in the limited time immediately after an external event and a predetermined period thereafter.

Background of the Invention

An integrated circuit or chip relies upon an external power source to perform its intended function. Typically, the external power source continuously provides power to the chip, even though the chip may not require the power at all times. As a result, the power source may be unnecessarily depleted, as in the case of a battery. Preserving battery power is extremely important in many electronic applications. Prior art attempts to preserve battery power rely upon components external to the chip. These components are relatively expensive and inconvenient to install.

Objects and Summary of the Invention

Thus, it is a general object of the present invention to provide a method and apparatus for limiting the power consumed by integrated circuits.

It is a related object of the present invention to provide an integrated circuit which consumes power only when required, that is, in the limited time immediately after an external event and a predetermined period thereafter.

These and other objects are achieved by a power conserving integrated circuit. The integrated circuit is coupled to its external power supply only in response to an external event. An initial power connection is made in response to the external event. An element on the integrated circuit detects the initial power connection. After detecting the initial power connection, a switch internal to the integrated circuit is closed so as to couple the power supply to the integrated circuit for a predetermined period of time sufficient for a function to be executed by the integrated circuit. Afterwards, the connection is terminated and is not reinitiated until another external event. Therefore, power is consumed only when necessary, thereby preserving the power source.

Brief Description of the Drawings

Additional objects and features of the invention will be more readily apparent from the following detailed description and appended claims when taken in conjunction with the drawings, in which:

Figure 1 which depicts a power conserving integrated circuit in accordance with the present invention.

Figure 2 depicts an alternate embodiment of the circuit of Figure 1.

Figure 3 depicts an alternate embodiment of the circuit of Figure 1 which utilizes software for retriggering the counter.

Figures 4A and 4B depict an alternate embodiment of the present invention which includes Vcc switching.

Detailed Description of the Invention

Referring to Figure 1, a power conserving integrated circuit package 20 in accordance with the present invention is depicted. The package 20 includes an integrated circuit or chip 22 positioned within a housing 24. Housing 24 includes a plurality of pins 26 for coupling the integrated circuit 22 to external components. The external components send input signals to the integrated circuit 22. In response to the input signals, the integrated circuit 22 performs some function and generates output signals. Integrated circuit 22 is powered by a battery 28 which is coupled through pins 26.

In accordance with prior art techniques, battery 28 constantly provides power to the integrated circuit 22. This approach is problematic in that a constant power supply is provided while for most integrated circuits only intermittent power is required. As a result, power from the battery 28 is unnecessarily depleted. In almost all circumstances, conservation of battery power is highly beneficial.

These problems are avoided in accordance with the teachings of the present invention. With the present invention, power is consumed intermittently: immediately after an external event and for a predetermined period thereafter. Consequently, power is only consumed when it is necessary; that is, power is consumed only when the integrated circuit 22 is executing a function. With the present invention, power consumption control is governed on board the chip, therefore, external components are not required to limit power consumption.

The benefits of this invention may be realized in the following manner. A plurality of switches 30 are coupled to the package 20 through pins 26. The switches monitor external events. An external event may be the touching of a button, a signal from an external circuit, or other analogous event occurring outside of the package 20. When an external event occurs which requires activity from integrated circuit 22, one of the switches 30 is momentarily closed and a closed circuit is formed from VCC to VSS through resistor 32, switch 30, line 33 and then NPN transistor 34.

Transistor 34 is a switch internal to the chip 22 that enables power to be connected or provided to

the internal circuitry of chip 22. When transistor 34 is open, the chip's internal VSS node 35 is left floating, and therefore will rise to approximately the same potential as the VCC node 36. When transistor 34 is closed, current flows through the transistor so as to maintain the VSS internal node 35 at approximately the same voltage potential as the VSS low potential node of battery 28. As will be understood by those skilled in the art, for MOS and CMOS integrated circuits, NPN transistor 34 would be replaced by either an NMOS transistor gated by lines 33 and 39, or a pair of complementary NMOS/PMOS transistors gated by the same signals and their complements.

The external activity which closes one of the switches 30 creates an initial connection which causes the transistor 34 to be turned on. Once the transistor 34 is turned on, node 35 is pulled low, allowing the circuitry inside the chip 22 to operate. This transition from a dormant to an active state is detected by activity monitor 37. Activity monitor 37 may be a transistor or other element which senses the presence of a current flowing through a transistor. Activity monitor 37 initializes counter 38 whenever a transition from a dormant to an active state is detected. As shown, signals derived from the external events will also be used by circuits internal to the chip 22.

The counter 38 outputs a signal on line 39 which enables a current to be provided to the base of transistor 34 for the predetermined period of time defined by the counter 38. Counter 38 will typically be a down counter that decrements from an initial value at a rate determined by an internally generated clock signal (not shown). Alternately, the counter 38 may be an RC circuit, having a predetermined decay rate, with a comparator which shuts off the supply of current to line 39 when an initial voltage level falls below a threshold level.

The "second power connection" provided via line 39 is needed to maintain power to the chip's internal circuitry because the switch 30 will toggle to its open position after being activated, which would cut the initial power connection to the chip. The second power connection effectively eliminates the problem of switch bouncing.

Transistor 34 will remain on during the duration of the period defined by the counter 38. As a result, power from the battery 28 will be available to any functional element 40 on the integrated circuit 22 during this period of time. Consequently, power will be available to the integrated circuit 22 from the time of an external event until a predetermined period thereafter as defined by the counter 38. This period of time will be sufficient to complete the function to be performed by the integrated circuit 22.

In the preferred embodiment, activity monitor 37 monitors at least some of the input event signals associated with switches 30, and resets counter 38 to its starting value each time that an external event signal is received. In this way, power will continue to be provided to the chip's internal circuitry until a predefined amount of time has elapsed after the last received event signal. This method of operation can be used to ensure that all event signals are processed before power to the chip is shut off, or to prevent unnecessary power-up and down cycles when a quick succession of external event signals are received.

Referring to Figure 2, in an alternate embodiment, transistor 34 is replaced by two switches or transistors 34 and 44. Transistor 34 forms the initial power connection whenever an external event signal is received, and transistor 44 is enabled by the counter's output signal on line 39 so as to maintain power to the chip 22 for a predetermined period of time. In either embodiment, the power is drawn from battery 28 only when required. This preserves the power in the battery.

Figure 3 depicts an alternate embodiment of the invention wherein the counter is reset by a software switch or trigger. Specifically, in the embodiment of Figure 3, a CPU circuit 50 senses transitions of the circuit 22 from a dormant to an active state, and when such a transition is detected it sends a reset signal to counter 38. As in above described embodiments, counter 38 maintains the circuit's power connection for a predetermined amount of time each time that it is reset. The CPU circuit 50 also monitors at least some of the input event signals associated with switches 30 and resets counter 38 to its starting value each time that an external event signal is received.

In addition, the CPU 50 relies upon memory 52 and stored software 54 to execute a given function. If the software 54 is executing a function which will not be completed in the period defined by the counter 38, then the software must include one or more in-line "counter reset" instructions to reset the counter 38. Each "counter reset" instruction in the software 54 causes CPU 50 to transmit a reset signal to the counter 38. As a result, power will be supplied to the chip 20 for a period sufficient to execute the given software function.

The embodiments disclosed herein switch ground or Vss. One skilled in the art will recognize that alternate embodiments are possible which entail switching Vcc. One suitable embodiment is disclosed in Figures 4A and 4B.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and

obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

Claims

1. A power conserving integrated circuit comprising:

   integrated switch means, internal to said integrated circuit, for coupling said integrated circuit to a power supply in response to an external event; and

   timing means, coupled to said integrated switch means, for maintaining said integrated switch means in a closed state so as to maintain a connection between said power supply and said integrated circuit only for a predetermined period after said external event.

2. The device of claim 1 wherein said timing means includes a counter for determining said predetermined period.

3. The device of claim 2 wherein said timing means includes means for re-initializing said counter in response to each said external event, whereby said integrated switch means maintains a connection between said power supply and said integrated circuit until said predetermined period has passed since a last one of said external events.

4. A power conserving integrated circuit comprising:

   integrated switch means, internal to said integrated circuit, for coupling said integrated circuit to a power supply only in response to an external event, said coupling of said power supply to said integrated circuit creating an initial power connection;

   activity monitoring means for detecting said initial power connection; and

   means, coupled to said activity monitoring means, for providing a second power connection between said power supply and said integrated circuit, said second power connection superseding said initial power connection and existing for a predetermined period after said initial power connection.

5. The apparatus of claim 4 wherein said providing means includes a counter.

6. A power conserving integrated circuit package comprising:

   a housing;

   an integrated circuit positioned within said housing, said integrated circuit including a power connecting transistor, a counter, an activity monitor, and at least one functional element; and

   a plurality of pins protruding from said housing and providing electrical connections between said integrated circuit and a plurality of external devices, said external devices including switches and a power supply, each of said switches being activated by an external event and causing an initial connection between said power supply and said power connecting transistor;

   wherein said activity monitor responds to said initial connection by generating signals which activate said power connecting transistor for a predetermined period of time as defined by said counter.

7. The power conserving integrated circuit package of claim 6 wherein said activity monitor includes means for responding to each activation of at least one of said external device switches by maintaining activation of said power connecting transistor until said predetermined period has passed since a last one of said external events.

8. A method of reducing the consumption of power by an integrated circuit, said method comprising the steps of:

   closing an integrated switch circuit, internal to said integrated circuit, so as to couple said integrated circuit to a power supply in response to an external event; and

   maintaining said integrated switch circuit in a closed state so as to maintain a connection between said power supply and said integrated circuit only for a predetermined period after said external event.

9. The method of claim 8, including the steps of

   detecting an initial power connection between said integrated circuit and said power supply after said external event; and

   creating a second power connection superseding said initial power connection, said second power connection coupling said power supply and said integrated circuit for a predetermined period after said initial power connection.

10. The method of claim 8, said maintaining step including:

responding to predefined external events which occur prior to termination of said predetermined period by maintaining said integrated switch circuit in a closed state until said predetermined period has passed since a last one of said external events.

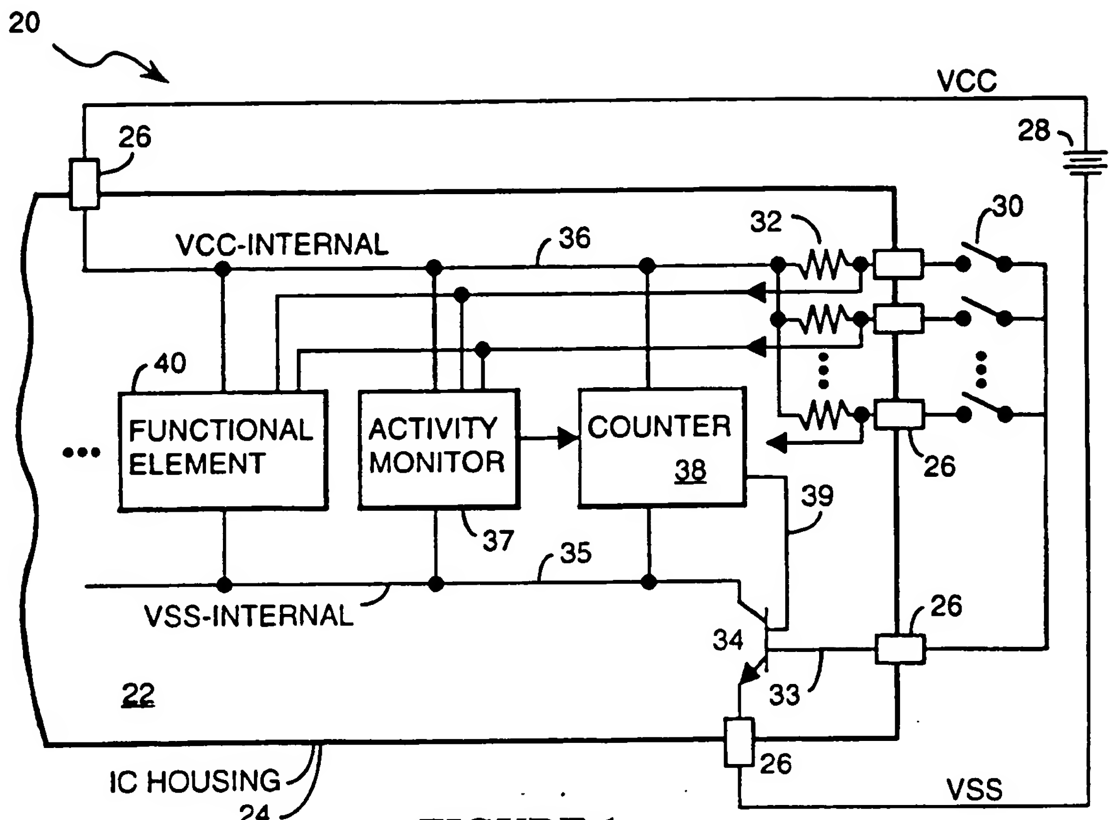

FIGURE 1

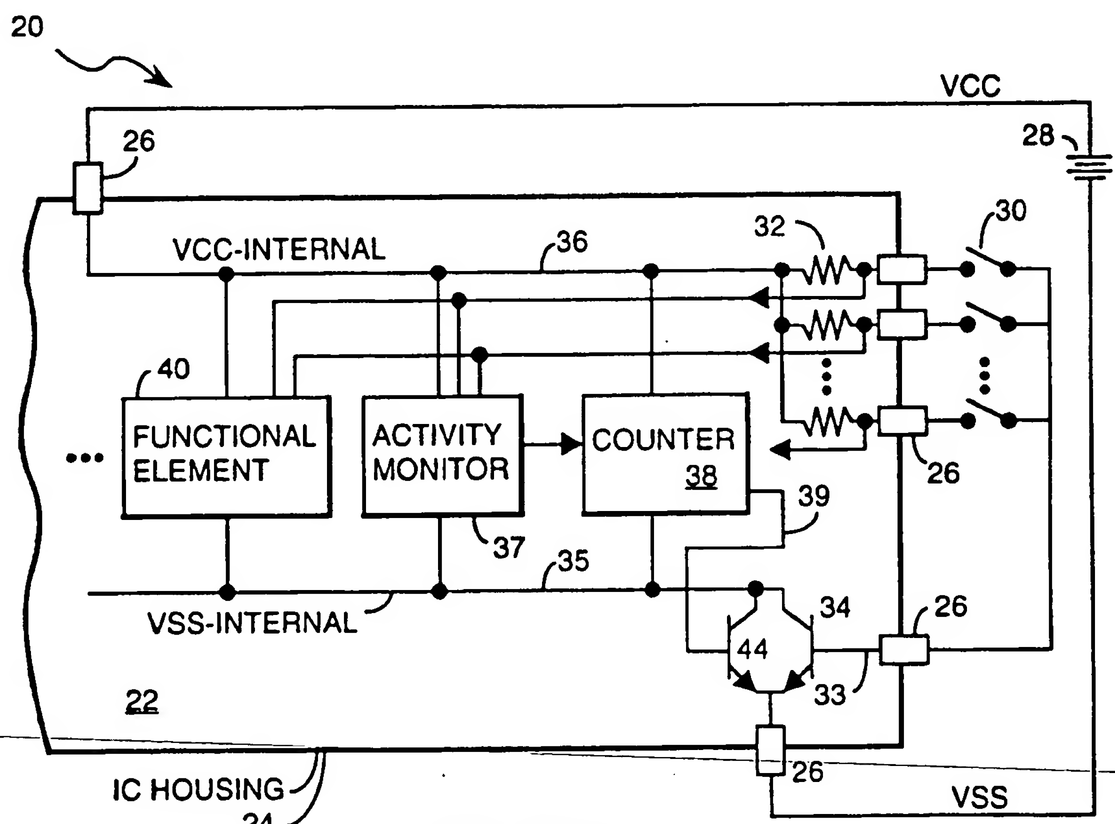

FIGURE 2

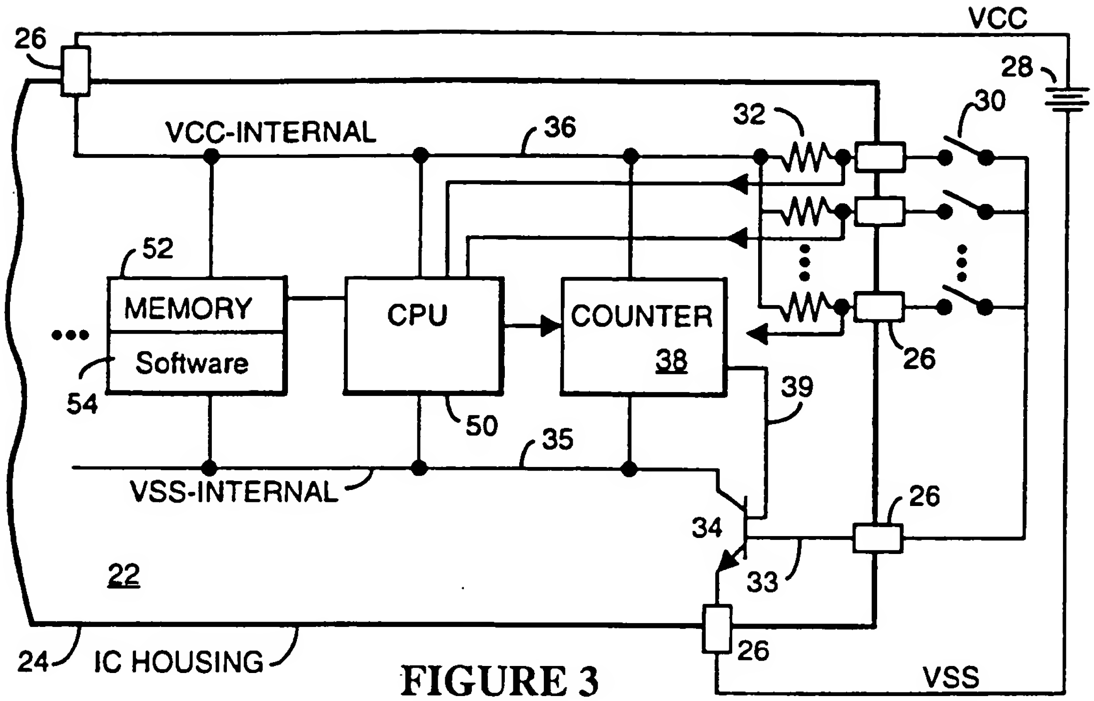

FIGURE 3

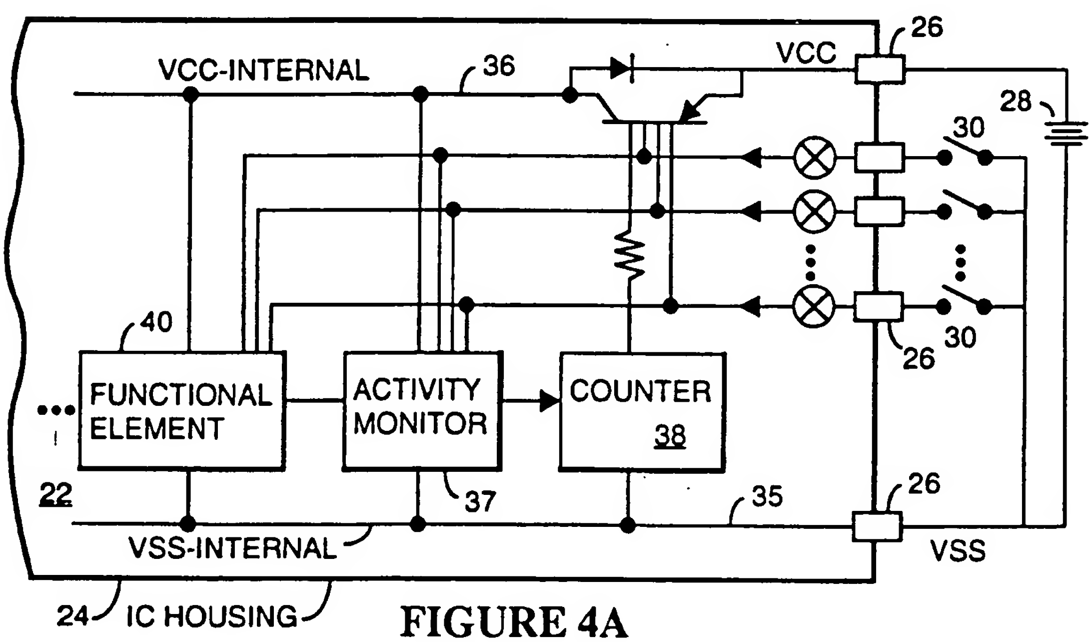

FIGURE 4A

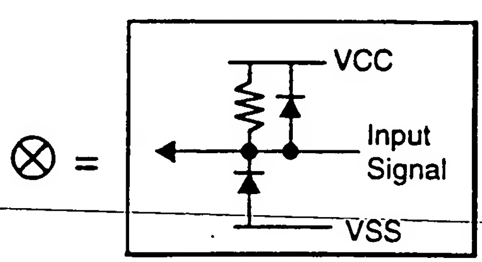

FIGURE 4B

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European Patent Office
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(11) Publication number: **0 549 165 A3**

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 92311063.9

(22) Date of filing: 03.12.92

(51) Int. Cl.5: H03K 17/94, H03K 17/28, H03K 19/00, G06F 1/32

(30) Priority: 23.12.91 US 813113

(43) Date of publication of application: 30.06.93 Bulletin 93/26

(84) Designated Contracting States: DE FR GB NL

(88) Date of deferred publication of the search report: 05.01.94 Bulletin 94/01

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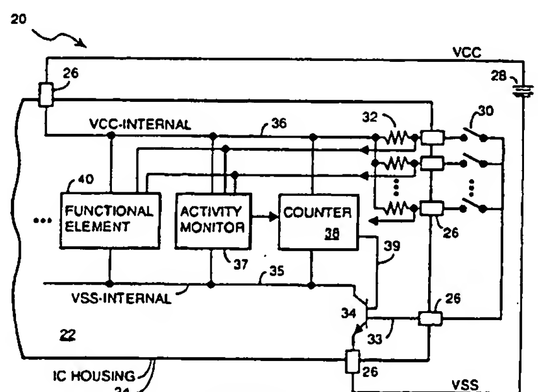

FIGURE 1

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EUROPEAN SEARCH REPORT

Application Number
EP 92 31 1063

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	US-A-4 279 020 (R. CHRISTIAN ET. AL.) * column 2, line 6 - line 64 * * column 4, line 37 - column 5, line 50; figures 1,3 *	1	H03K17/94 H03K17/28 H03K19/00 G06F1/32
X	DE-A-29 11 998 (BOSCH GMBH.) * page 5, line 26 - page 8, line 1; figure 1 *	4	
X,P	ELECTRONIC DESIGN NEWS vol. 37, no. 2 , 20 January 1992 , NEWTON, US page 133 C. HALLMAN 'Battery Powered Microprocessor Turns Itself Off' * page 133, column 2, line 3 - line 15; figure 1 *	1	
A	US-A-3 736 569 (W. BOURICIUS ET. AL.) * column 1, line 35 - line 55; claims 4,5 *	1,2	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H03K
G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 November 1993	BUTLER, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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